SPECIFICATION

Amendments to the Specification:

Please replace the paragraph beginning at page 5, line 21 with the following amended paragraph:

With reference to Figure 2C, the input signal is shown applied to the I/O pad P through the transmission line represented by the impedance Z_L. The tracking system employs a capacitor [[~~C_T~~ C_r]] having one terminal coupled to one terminal of the parasitic capacitance C_P and the other terminal coupled between a current source 12 and an NMOS transistor 14 having its gate coupled its drain, as well as with the gate of the second NMOS transistor 16. A PMOS transistor 18 has its drain and gate coupled to a drain of NMOS transistor 16 as well as with the gate of the second PMOS transistor 20.

Please replace the paragraph beginning at page 5, line 28 with the following amended paragraph:

In operation, during a rising edge signal (+dv/dt), since the voltage of [[~~C_T~~]] [[C_r]] cannot change instantaneously, the voltage increases at terminal 22 which ultimately causes the drain of PMOS transistor 20 to provide sufficient current at terminal 24 to compensate for a portion of the current that would otherwise be provided to parasitic capacitance [[~~C_T~~]] [[C_P]] by the input signal.